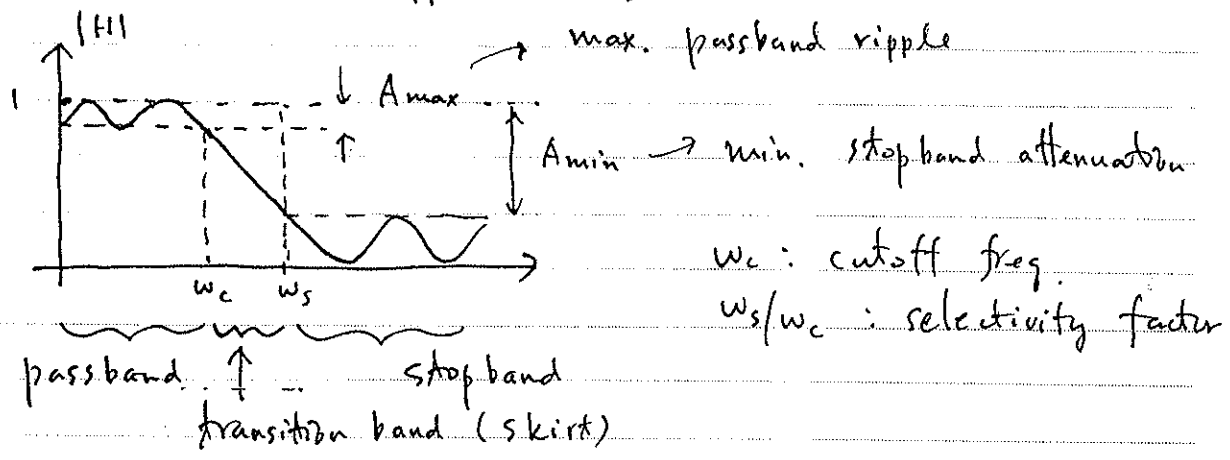


Chapter 4 Active filters : Part II

- Sharp cutoff \Rightarrow higher order filter (continuous-time)
 - [Cascade design
 - direct synthesis
- Switched capacitor filter { sampled data system
audio signal processing

4.1 Filter Approximations



ω_c : cutoff freq.
 ω_s/ω_c : selectivity factor

$A(\omega) = -20 \log_{10} |H(j\omega)|$: attenuation

- polynomial approximation {
- Butterworth
 - Chebyshev
 - Cauer elliptic
 - Bessel

Design procedure

- ① Filter spec. ($\omega_c, \omega_s, A_{max}, A_{min}$)
- ② Find required order n (handbook or $S(\omega)$)

③ $\left\{ \begin{array}{l} \text{Cascade approach, or} \\ \text{RLC ladder approach} \end{array} \right.$

③ $\left\{ \begin{array}{l} \omega_c, \theta \text{ for each stage, or} \\ \text{R, L, C} \end{array} \right.$

* Butterworth approximation (maximally flat)

$$H(j\omega) = \frac{1}{\sqrt{1 + \varepsilon^2 (\omega/\omega_c)^{2n}}}$$

- n : order
- ω_c : cutoff freq.
- $A_{\max} = A(\omega_c) = 20 \log_{10} \sqrt{1 + \varepsilon^2} = 10 \log_{10} (1 + \varepsilon^2)$
- maximally flat, slow roll-off
- roll-off: $-20n$ dB/dec (stopband)
- Fig 4.4 (a)
- Example 4.1

* Chebyshev approximation

$$H(j\omega) = \frac{1}{\sqrt{1 + \varepsilon^2 C_n^2(\omega/\omega_c)}}$$

Chebyshev

polynomial $\leftarrow C_n(\omega/\omega_c \leq 1) = \cos [n \cos^{-1}(\omega/\omega_c)]$
 $C_n(\omega/\omega_c \geq 1) = \cosh [n \cosh^{-1}(\omega/\omega_c)]$

$C_n(\omega/\omega_c)$

- max. roll-off } ripple $\uparrow \rightarrow$ roll-off \uparrow
- passband ripple
- ω_c : cutoff freq.
- $A_{\max} = 10 \log_{10} (1 + \varepsilon^2)$
- ultimate roll-off = $-20n$ dB/dec. \rightarrow ultimate
- Fig 4.4 (b)

* Cauer approximation

- Cauer filter or elliptic filter
- ripples in both passband and stopband
- sharper roll-off
- Fig 4.5

* Bessel approximation

- Bessel filter or Thomson filter
- maximize passband delay \Rightarrow linear phase in passband
- less sharp roll-off
- Fig. 4.6

4.2 Cascade Design

$$H(s) = H_1(s) H_2(s) \dots H_{n/2}(s) \quad : \text{if } n \text{ is even}$$

* Lowpass filter design

Table 4.1

f_0 : normalized freq. (1 Hz)

$\begin{cases} f_0 = -1 \text{ dB cutoff freq. for Butterworth \& Bessel} \\ f_0 = \text{edge of ripple band for Chebyshev \& Cauer} \end{cases}$

$f_{1,2} = f_{2,1} = f_c$

$$\begin{cases} f_0 = f_0(\text{table}) \times f_c \\ f_2 = f_2(\text{table}) \times f_c \end{cases}$$

- ⊙ Example 4.2 : 30 kHz . (Fig 4.7, 4.8)
- ⊙ Example 4.3 : 30 kHz . (Fig 4.9)

pl11 → pl49

* Highpass Filter Design

- $s/\omega_c \rightarrow 1/(s/\omega_c)$
- (LP \rightarrow HP) $H(s)$ into $1/H(s)$
- LP \rightarrow Table with
- $$\begin{cases} f_0 = f_c / f_0(\text{table}) \\ f_2 = f_c / f_2(\text{table}) \end{cases}$$

- ⊙ Example 4.4 (Fig 4.10)

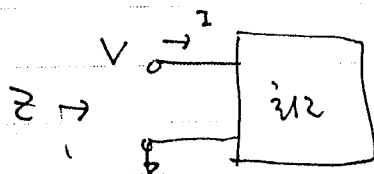
* Bandpass Filter Design

- ⊙ Example 4.5 (Fig 4.11)
- ⊙ Example 4.6 (Fig 4.12)

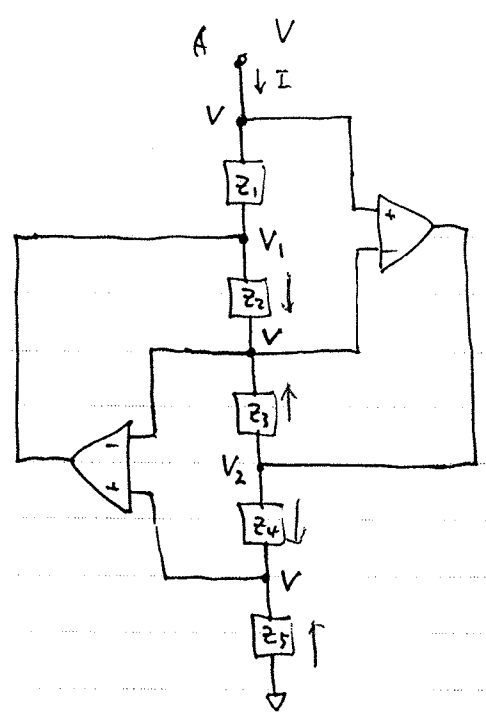
* Band reject Filter Design

- ⊙ Example 4.7

4.3 Generalized Impedance Converters (GIC)



$$Z = \frac{V}{I}$$



$$I = \frac{V - V_1}{Z_1}$$

$$\frac{V_1 - V}{Z_2} + \frac{V_2 - V}{Z_3} = 0$$

$$\frac{V_2 - V}{Z_4} + \frac{0 - V}{Z_5} = 0$$

$$\Downarrow$$

$$Z = \frac{V}{I} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$$

① $Z_1 = R_1, Z_2 = 1/j\omega C_2, Z_3 = R_3, Z_4 = R_4, Z_5 = R_5$

$$Z = \frac{R_1 R_3 R_5}{(1/j\omega C_2) R_4} = j\omega \frac{R_1 R_3 R_5 C_2}{R_4} = j\omega L$$

⇒ grounded inductance

② $Z_1 = 1/j\omega C_1, Z_2 = R_2, Z_3 = R_3, Z_4 = R_4, Z_5 = 1/j\omega C_5$

$$Z = -\frac{1}{\omega^2 D}, \quad D = \frac{R_2 R_4 C_1 C_5}{R_3}$$

⇒ grounded FPNR (freq-dependent negative resistance)

OR D element

Fig 4.16 \Rightarrow D-element = Σ 다른 Σ 이

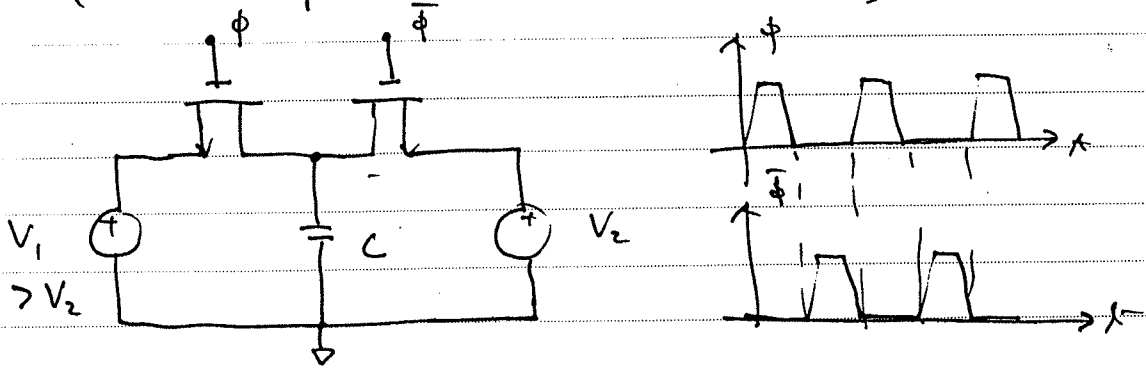
* Synthesis using grounded inductances
Example 4.8 (Fig 4.17)

* Synthesis using FDNR

4.4 Direct Design

4.5 Switched Capacitor Filter (SC Filters)

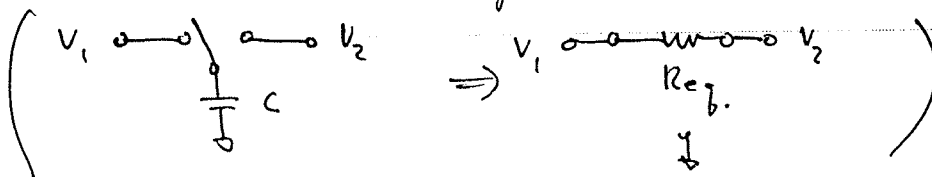
{ Mos cap. + MOSFET switch } simulate cap.



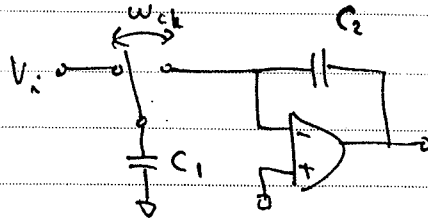
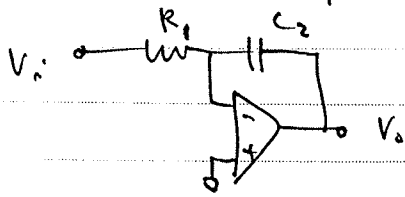
$$\Delta Q = C(V_1 - V_2)$$

$$I_{avg} = C f_{clk} (V_1 - V_2) = \Delta Q \cdot f_{clk} = \frac{\Delta Q}{\Delta t}$$

$$\Rightarrow R_{eq} = \frac{V_1 - V_2}{I_{avg}} = \frac{1}{C f_{clk}}$$



* SC Integrator



$$H(j\omega) = \frac{-1}{j\omega/R_1 C_2}$$

$w_{ck} \gg \omega$ (input signal freq.)

$$\omega_0 = \frac{1}{R_1 C_2}$$

$$\omega_0 = \frac{1}{R_{eq} C_2} = \frac{C_1}{C_2} f_{ck}$$

< SC 의 설계 >

- ① R 이 작을수록 \rightarrow 칩 표면 증대 비용
- ② C_1/C_2 는 0.1% 를 지니도록
- ③ ω_0 가 f_{ck} 에 비례 하도록 ω_0 는 지니도록 설계

- C 는 $\geq 0.1 \text{ pF} \sim 100 \text{ pF}$ 범위 (1 pF ~ 10 pF 는 24.25 pF 이므로 사용 안 함)

- 설계 자료 : Fig 4.26

4.6 Switched Capacitor filter

Fig 4.29

Fig 4.30

H/w

- 4-6, ~~4-7, 4-8, 4-9~~, 4-10, 4-18, 4-19, 4-22,