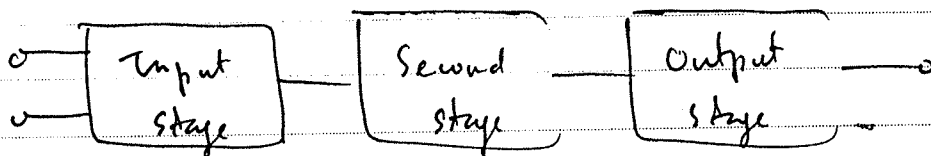


Chapter 5 Static Op Amp. Limitations

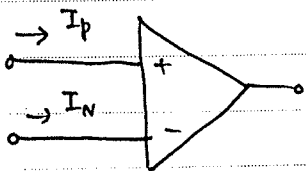
← Fig 5.1

- I_B : input bias current
- I_{os} : " offset "
- V_{os} : " " voltage
- $e_{n, in}$: ac noise density
- $TC(V_{os})$: thermal drift
- CMRR
- PSRR : power supply rejection ratio
- gain nonlinearity

5.1 Op Amp Circuit Diagram



5.2 Input Bias and Offset Current



- $I_p \neq 0$, $I_n \neq 0$, $I_p \neq I_n$ (due to mismatch)
- DC bias currents
- Both input terminals must have a dc path so that I_p and I_n can flow
- $\begin{cases} I_p \text{ \& } I_n > 0 & \Leftarrow \text{ npn BJT, p-channel FET} \\ I_p \text{ \& } I_n < 0 & \Leftarrow \text{ pnp BJT, n-channel FET} \end{cases}$

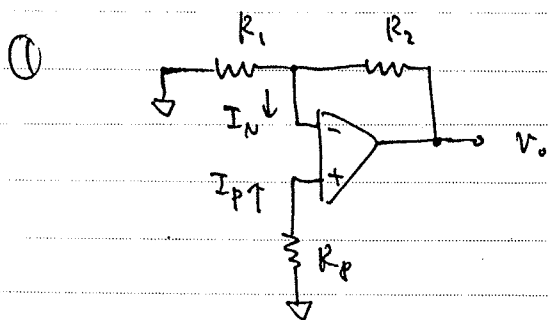
$$\left\{ \begin{array}{l} I_B = \frac{I_p + I_N}{2} \quad : \text{input bias current} \\ I_{os} = I_p - I_N \quad : \text{input offset current} \end{array} \right.$$

($I_{os} \ll I_B$ in general)

$$\left\{ \begin{array}{l} I_B \text{ in } \mu\text{A} \sim \text{fA} \\ I_{os} \text{ in } \text{nA} \sim \text{fA} \end{array} \right.$$

I_B & I_{os} are temperature dependent
(Fig 5A8, 5A9 p 259, p 260)

* Errors Caused by I_B and I_{os}



$$V_p = -R_p I_p$$

$$I_p \rightarrow \text{is } I_N \quad V_N = R_2 I_N$$

$$\begin{aligned} V_o &= \left(1 + \frac{R_2}{R_1}\right) V_p + R_2 I_N \quad (\text{by superposition}) \\ &= R_2 I_N - \left(1 + \frac{R_2}{R_1}\right) R_p I_p \\ &= \left(1 + \frac{R_2}{R_1}\right) \left[(R_1 \parallel R_2) I_N - R_p I_p \right] \\ &= E_o \quad : \text{output dc noise} \end{aligned}$$

$(R_1 \parallel R_2) I_N - R_p I_p$: input dc noise

$\left(1 + \frac{R_2}{R_1}\right)$: dc noise gain

$$V_o = E_o = \left(1 + \frac{R_2}{R_1}\right) \left[\left\{ (R_1 \parallel R_2) - R_p \right\} I_B - \left\{ (R_1 \parallel R_2) + R_p \right\} I_{os}/2 \right]$$

If $R_p = (R_1 \parallel R_2)$,

$$E_o = \left(1 + \frac{R_2}{R_1}\right) \left(-R_1 \parallel R_2 \right) I_{os}$$

Q E_o 가 I_{os} 에 비례

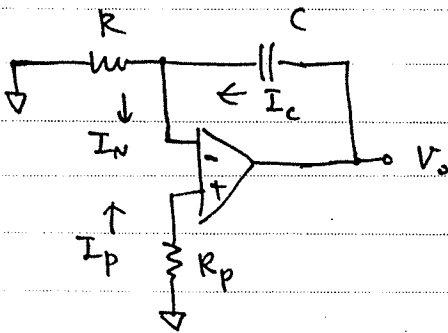
① $R_p = R_1 \parallel R_2$

② I_{os} 가 I_B 에 비례 op amp 이득

③ R_1 과 R_2 는 I_{os} 에 비례 $I_B = I_{os}$ 가 되게 하려면 $I_B = I_{os}$ (이때는 I_{os} 가 I_B 가 되도록 하려면 $I_B = I_{os}$)

① Example 5.1

②



$$V_N = V_P = -R_p I_P$$

$$\frac{V_N}{R} + I_N - I_C = 0$$

$$I_C = \frac{1}{R} (R I_N - R_p I_P) = \frac{1}{R} \left[(R - R_p) I_B - (R + R_p) I_{os}/2 \right]$$

$$V_o(t) = E_o(t) + V_o(0)$$

$$= \frac{1}{R_c} \int_0^t \left[(R - R_p) I_B - (R + R_p) I_{os}/2 \right] d\xi$$

input error
output error + $V_o(0)$

$$E_o(t) \approx \left[(R - R_p) I_B - (R + R_p) I_{os}/2 \right] t / R_c$$

→ ramp → tends to saturate op amp.

① $E_o(t) = 1$ 원하는 값

① $R_p = R \Rightarrow E_o(t) = \frac{1}{R_c} \int_0^t -R I_{os} dt$

② I_{os} 원하는 값 of amp 원하는 값

① Example 5.2

① Summary

- ① $R_{\text{seen by } I_p} = R_{\text{seen by } I_n}$
- ② 가장 작은 값은 R 원하는 값
- ③ $I_{os} \approx$ 원하는 값 of amp 원하는 값

5.3 Low-Input-Bias-Current op amp.

* Superbeta-Input op amp

- LM 308 (NS)
- $I_B \approx 1 \text{ nA}$ or less

* Input-Bias-Current Cancellation

- op-07 (AD)
- $I_B = \pm 1 \text{ nA}$, $I_{os} = 0.4 \text{ nA}$

* JFET-Input op amp.

- $\left\{ \begin{array}{l} \text{LF 356} \\ I_B = 30 \text{ pA} \end{array} \right.$: bi FET op amp (NS)
- $\left\{ \begin{array}{l} \text{AD 549 (AD)} \\ I_B < 100 \text{ fA} \end{array} \right.$, OPA129 (BB)

(212 222, 22222)

- Applications : electrometer, ion gauge, photo detector

* MOSFET-Input Op Amp.

- TLC 279 : CMOS op amp (TI)
 $I_B = 0.7 \text{ pA}$, $I_{os} = 0.1 \text{ pA}$

* Input Bias-Current Drift : Fig 5.9

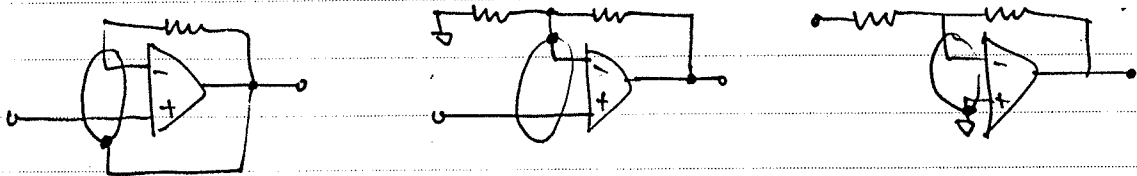
- BJT : $T \uparrow \Rightarrow I_B \downarrow$

- FET : $T \uparrow \Rightarrow I_B \uparrow$

* Input Guarding : Fig 5.10

- Guard ring minimizes leakage current across PCB

- Use Teflon sockets if any



5.4 Input Offset Voltage : Fig 5.11

$$- v_o = a(v_p - v_n) \neq 0 \text{ for } v_p = v_n$$

$$- v_o = a(v_p + V_{os} - v_n) = 0, \text{ OR}$$

$$v_n = v_p + V_{os}$$

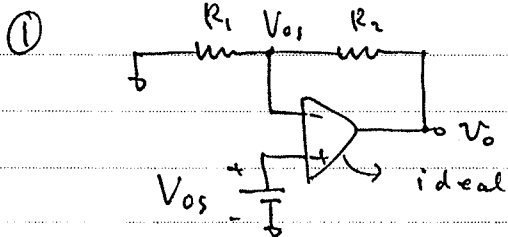
input offset voltage

$$(\Rightarrow v_n \neq v_p)$$

- V_{os} : $mV \sim \mu V$

- 741C : $V_{os} = 2mV \sim 6mV$
 - 741E : $V_{os} = 0.8mV \sim 3mV$
 - OP-27 : $V_{os} = 10\mu V \sim 50\mu V$
- ↳ ultralow offset voltage of amp.

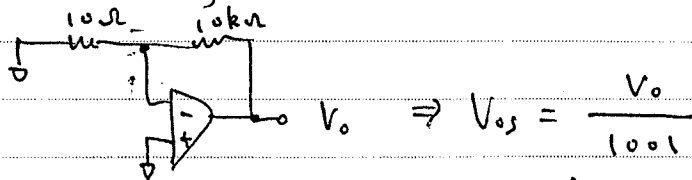
* Errors Caused by V_{os}



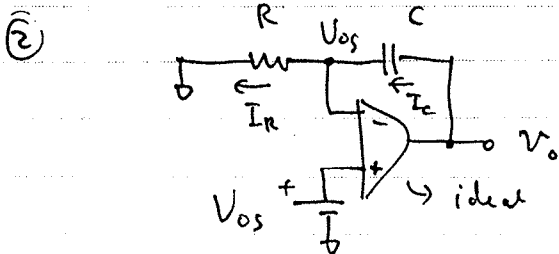
$$v_o = E_o = \left(1 + \frac{R_2}{R_1}\right) V_{os}$$

- $\left(1 + \frac{R_2}{R_1}\right)$: dc noise gain

- Measurement of V_{os}



$$\left(R_1 \parallel R_2 \approx R_2 \quad I_B = 1 \mu A \text{ at } 25^\circ C\right)$$



$$I_c = I_R = \frac{V_{os}}{R}$$

$$v_o(t) = E_o(t) + v_o(0) = \frac{1}{Rc} \int_0^t V_{os} dt + v_o(0)$$

- ramp \Rightarrow of amp saturation

* Thermal Drift

- $TC(V_{os}) = \frac{\partial V_{os}}{\partial T} \sim \mu V/^{\circ}C$

- 741 : $TC(V_{os}) \sim 5 \mu V/^{\circ}C$

- op-77 : $TC(V_{os}) \sim 0.1 \mu V/^{\circ}C \sim 0.3 \mu V/^{\circ}C$

$V_{os}(T) \doteq V_{os}(25^{\circ}C) + TC(V_{os})_{avg} \times (T - 25^{\circ}C)$

* CMRR

- $v_o = a_{dm}(v_p - v_n) + a_{cm}v_{cm}$

$\begin{cases} a_{dm}: \text{differential-mode gain} = a \\ a_{cm}: \text{common-mode gain} \\ v_{cm} = \frac{1}{2}(v_p + v_n) \end{cases}$

$v_o = a_{dm} \left[v_p - v_n + \frac{a_{cm}}{a_{dm}} v_{cm} \right]$

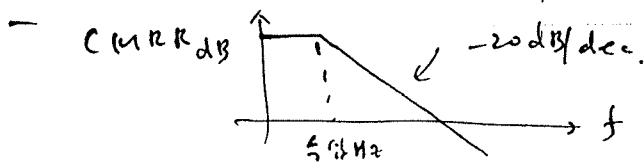
$= a_{dm} \left[v_p + \underbrace{\frac{v_{cm}}{CMRR}} - v_n \right]$

↳ input offset voltage v_{ic} .

$(CMRR)^{-1} = \frac{\partial V_{os}}{\partial v_{cm}} = 10^{-\frac{CMRR_{dB}}{20}}$

$(CMRR_{dB} = 20 \log_{10} CMRR)$

- 741 : $CMRR_{dB} = 70 \sim 90 \text{ dB}$ $\nearrow (CMRR)^{-1}: 31.6 \sim 316 \mu V/V$
- op-77 : $(CMRR)^{-1} = 0.1 \sim 1 \mu V/V$



- Since $V_N \approx V_P$, $V_{cm} \approx V_P = V_N$
- Inverting amp $\Rightarrow V_P = 0 \Rightarrow CMRR \approx \frac{2}{a} \frac{1}{\delta V_N}$
- IA $\Rightarrow CMRR \approx \frac{2}{a}$

⊙ Example 5.4

* PSRR (Power Supply Rejection Ratio)

- $\frac{\partial V_o}{\partial V_s} =$ 전압 δV_s 이차 V_s 가 δV_s 이차

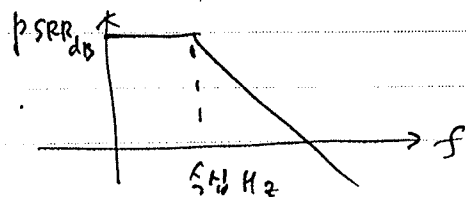
↓

input offset voltage 이차

$$V_o = a \left[V_P + \frac{\delta V_s}{PSRR} - V_N \right]$$

$$\frac{1}{PSRR} = \frac{\partial V_o}{\partial V_s} \quad \text{in } \mu\text{V/V}$$

- PSRR : $A_{VO} \sim 120 \text{ dB}$
- 741 : $(PSRR)^{-1} = 30 \sim 150 \mu\text{V/V}$
- op-77 : $(PSRR)^{-1} = 0.7 \sim 3 \mu\text{V/V}$



- 60Hz ripple or high-freq ripple in switching mode power supply

↓

δV_s

↓

V_{os}

\Rightarrow output noise (hum $\frac{C}{S}$)

↑

⊙ Example 5.5

- * Change of V_{os} with Output Swing
 - a is finite $\Rightarrow \Delta v_o$ produces $\Delta v_o/a$ at input

$$v_o = a \left[v_p + \underbrace{\frac{\Delta v_o}{a}}_{\Delta V_{os}} - v_n \right]$$

Summary:

$$V_{os} = \underbrace{V_{os0}}_{\text{initial input offset voltage}} + TC(V_{os}) \Delta T + \frac{\Delta v_p}{CMRR} + \frac{\Delta v_s}{PSRR} + \frac{\Delta v_o}{a}$$

③ Example 5.6

5.5 Low-Input-Offset-Voltage Op Amp.

* Bipolar Op Amp

- op-27E (AD) : $V_{os} = 10 \mu V \sim 25 \mu V$
 $TC(V_{os}) = 0.2 \mu V/^\circ C \sim 0.6 \mu V/^\circ C$

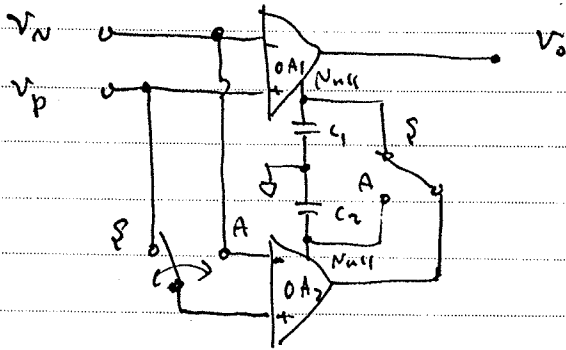
* FET-Input Op Amp

- AD547L (AD) : $V_{os} = 250 \mu V$
 $TC(V_{os}) \leq 1 \mu V/^\circ C$

- OPA627B (BB) : $V_{os} = 40 \mu V$
 $TC(V_{os}) = 0.4 \mu V/^\circ C$

- LT1055A (LT) : $V_{os} = 50 \mu V$
 $TC(V_{os}) = 1.2 \mu V/^\circ C$

* Chopper - stabilized Op Amp (CSOA)
 - Auto zero op amp.



$\left\{ \begin{array}{l} S: \text{ sampling} \\ A: \text{ auto-zero} \end{array} \right.$
 Switching: $5 \mu\text{s}$ Hz
 internal oscillator

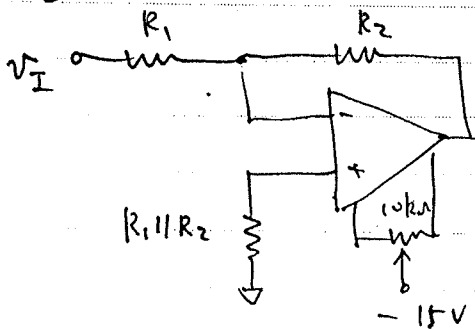
- Auto-zero mode: OA2 2MHz , $V_{OS2} \frac{1}{2} \mu\text{V}$
- Sampling mode: OA1 1MHz , $V_{OS1} \frac{1}{2} \mu\text{V}$

- LTC1050 (LT) : $V_{OS} = 0.5 \mu\text{V}$, $TC(V_{OS}) = 0.01 \mu\text{V}/^\circ\text{C}$
- MAX420 (Maxim) : $V_{OS} = 1 \mu\text{V}$, $TC(V_{OS}) = 0.02 \mu\text{V}/^\circ\text{C}$

↙ - Switching noise, freq. aliasing problem

5.6 Input Offset - Error Compensation

(1)



$$v_o = A_s v_i + E_o$$

$$E_o = \left(1 + \frac{R_2}{R_1}\right) [V_{OS} - (R_1 || R_2) I_{OS}]$$

$$= \frac{1}{3} E_I$$

Fig 5.11 (a) $\frac{1}{3} E_I$
 (b) $\frac{1}{3} E_I$

$$A_s = -\frac{R_2}{R_1} \quad \text{or} \quad 1 + \frac{R_2}{R_1}$$

↳ signal gain

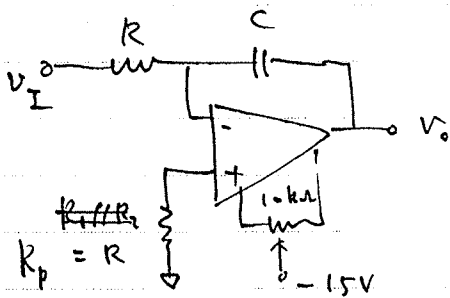
$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}$$

" V_{os} or I_{os} 가 입력에 $\frac{1}{\beta}$ 만큼
증가하면 출력은 $\frac{1}{\beta}$ 만큼
증가한다."

$E_I = V_{os} - (R_1 || R_2) I_{os}$: total offset error referred to the input

E_o : total offset error referred to the output

②



$$V_o(t) = -\frac{1}{RC} \int_0^t [V_I(\xi) + E_I] d\xi + V_o(0)$$

$$E_I = R I_{os} - V_{os}$$

* Internal Offset Nulling

- External trimmer : 입력 저항, 이득 저항, 출력 저항을
만든다.

(Fig 5.3 은 10kΩ 가 저항 사용)

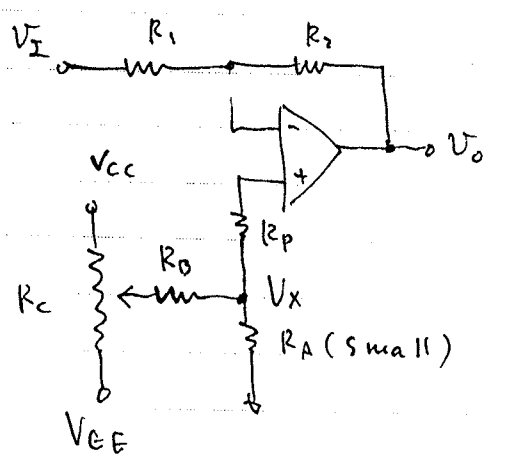
- Calibration : ① set $V_I = 0$
② Adjust trimmer for $V_o = 0$

- Dual or quad op amp package 는 internal nulling 기능을 제공한다. (\because pin 수가 적기 때문)

↓
trimmer 는 1개 인 internal nulling 은 2개 이므로
그러한 pin 은 2개 인 op amp 는 2개 이다.

* External Offset Nulling

- 외부에서 입력 저항을 조정하여 nulling.
- CMRR, PSRR, drift 등 $\frac{V_o}{V_{in}}$ 에 영향을 줄 수 있는 것들을 많이.

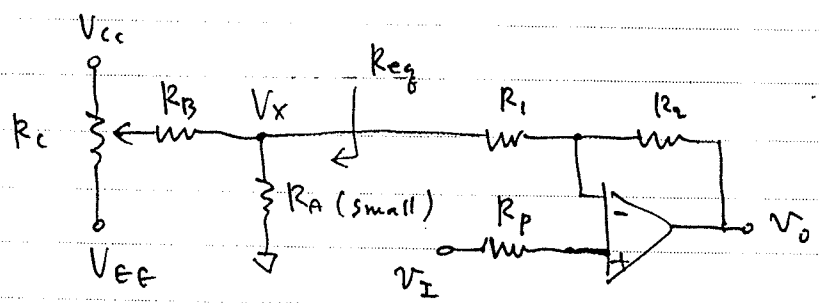


(Integrator에 비해서 R2 채널)

$$\begin{cases} R_B \gg R_C \\ R_A \ll R_P \end{cases}$$

- calibration

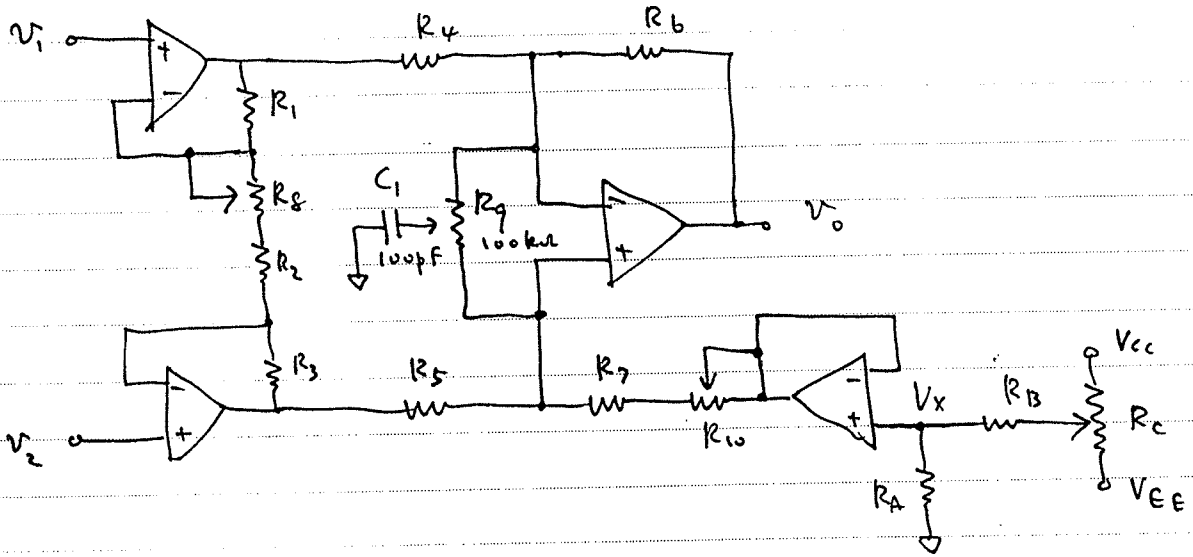
- 1) $V_I = 0$
- 2) Adjust R_B for $V_O = 0$



$$\begin{cases} R_{eq} \ll R_1 \\ R_A \ll R_B \Rightarrow R_{eq} \approx R_A \end{cases}$$

$$A_s = 1 + \frac{R_2}{R_{eq} + R_1}$$

② 3-op amp IA



- ① v_1 and $v_2 = 0$ (grounded) 이어서 R_c 를 조절하여 $v_o = 0$
- ② R_8 을 조절하여 $A_{DM} = \frac{v_o}{v_I}$
- ③ $v_1 = v_2 = v_I$, $-10V \leq v_I \leq 10V$ 이어서 v_o 가 최소가 되도록 R_{10} 조절 (max. dc CMRR)
- ④ $v_1 = v_2 = v_I$, $v_I =$ 제 1번 T_A 이어서 v_o 가 최소가 되도록 R_9 조절.
 (이때 $10kHz$ 정도이면 C_1 은 $100pF$ 충분)
 C_1 은 R_9 이 커지면 short 이 되어가므로 조절 필요)
 AC CMRR

5.7 Maximum Ratings

- operating Temp

}	Commercial range	: $0 \sim 70^\circ C$
	Industrial	: $-25 \sim 85^\circ C$
	Military	: $-55 \sim 125^\circ C$

* Absolute Maximum Ratings

- If exceeded, permanent damage.
- Maximum supply voltages
- Maximum differential-mode input voltages
- " Common-mode " "
- Maximum internal power dissipation (P_{max})

* Input Voltage Range

- input voltage range for normal operation
- single-supply op amp ($V_{SS} = -1.5V \sim 0V$): LM324 (NS)

* Output Voltage Swing

- $V_{OL} \leq V_o \leq V_{OH}$
- rail-to-rail op amp: LMC664x (NS)
 $\hookrightarrow V_{EE} \leq V_o \leq V_{CC}$

* Overload Protection

- I_{sc} : output short-circuit current
- 741: $I_{sc} \doteq 25 \text{ mA}$
- power op amp
 PA04 (Apex Microtechnology): 20 A
 OPA501 (BB): 10 A

H/W: 5.2, 5.7, 5.10, 5.12, 5.23, 5-29