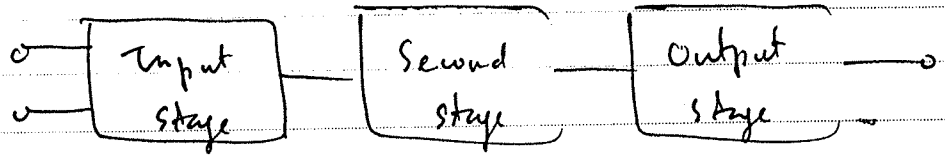
Chapter 5 Static Op Amp. limitations

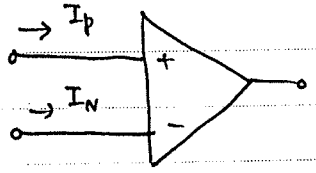
← Fig 5.1

- I_B : input bias current
- I_{OS} : " offset "
- V_{OS} : " " voltage
- e_n, i_n : ac noise density
- TC(V_{OS}) : thermal drift
- CMRR
- PSRR : power supply rejection ratio
- gain nonlinearity

5.1 Op Amp Circuit Diagram



5.2 Input Bias and Offset Current



- $I_P \neq 0$, $I_N \neq 0$, $I_P \neq I_N$ (due to mismatch)
- DC bias currents
- Both input terminals must have a dc path so that I_P and I_N can flow
- $\begin{cases} I_P \text{ \& } I_N > 0 \in \text{npn BJT, p-channel FET} \\ I_P \text{ \& } I_N < 0 \in \text{pnp BJT, n-channel FET} \end{cases}$

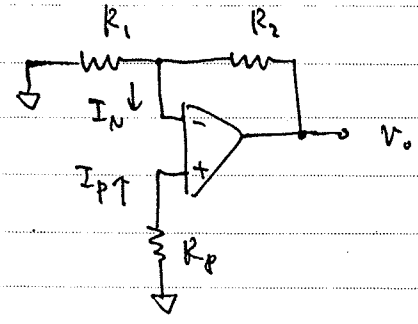
$$\begin{cases} I_B = \dfrac{I_p + I_N}{2} & : \text{input bias current} \\ I_{os} = I_p - I_N & : \text{input offset current} \end{cases}$$

($I_{os} \ll I_B$ in general)

$$\begin{cases} I_B \text{ in } & nA \sim fA \\ I_{os} \text{ in } & nA \sim fA \end{cases}$$

I_B & I_{os} are temperature dependent
(Fig 5A8, 5A9 p259, p260)

* Errors Caused by I_B and I_{os}

① 

$V_p = -R_p I_p$

$I_p = 0$ then $V_N = R_2 I_N$

$$\begin{aligned} V_o &= \left(1 + R_2/R_1\right) V_p + R_2 I_N \qquad \text{(by superposition)} \\ &= R_2 I_N - \left(1 + R_2/R_1\right) R_p I_p \\ &= \left(1 + \frac{R_2}{R_1}\right)\left[\left(R_1 \| R_2\right) I_N - R_p I_p \right] \\ &= E_o \qquad : \text{output dc noise} \end{aligned}$$

$(R_1 \| R_2) I_N - R_p I_p$: input dc noise

$\left(1 + \frac{R_2}{R_1}\right)$: dc noise gain

$$V_o = E_o = \left(1+\frac{R_2}{R_1}\right)\left[\{(R_1 \| R_2) - R_p\} I_B - \{(R_1 \| R_2) + R_p\} I_{os}/2\right]$$

If $R_p = (R_1 \| R_2)$,

$$E_o = \left(1+\frac{R_2}{R_1}\right)\left(-R_1 \| R_2\right) I_{os}$$

② E_o 의 특징

① $R_p = R_1 \| R_2$

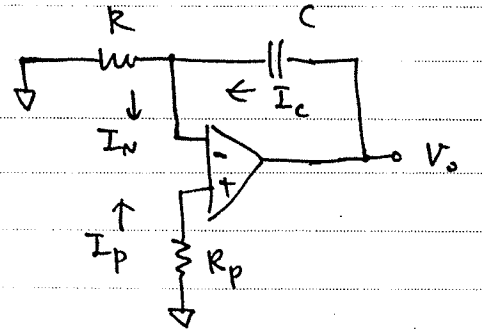
② I_{os} 가 작은 op amp 사용

③ R_1 과 R_2 는 작은 값의 저항을 사용

(이때는 정밀 오차 증폭하므로 주의)

③ Example 5.1

④



$$V_N = V_p = -R_p I_p$$

$$\frac{V_N}{R} + I_N - I_c = 0$$

$$I_c = \frac{1}{R}\left(R I_N - R_p I_p\right) = \frac{1}{R}\left[(R-R_p) I_B - (R+R_p) I_{os}/2\right]$$

$$V_o(t) = E_o(t) + V_o(0)$$

$$= \frac{1}{Rc}\int_0^t \underbrace{\left[(R-R_p) I_B - (R+R_p) I_{os}/2\right]}_{\text{input error}} d\xi + V_o(0)$$

output error

$$E_o(t) \simeq \left[(R - R_p) I_B - (R + R_p) I_{os}/2 \right] t / RC$$

→ ramp → tends to saturate op amp.

⑧ $E_o(t)$ = 일정한 값

① $R_p = R \Rightarrow E_o(t) = \frac{1}{RC} \int_0^t -R I_{os}\, d\xi$

② I_{os} 가 작은 op amp 사용

⑨ Example 5.2

⑩ Summary

① $R_{seen\ by\ I_p} = R_{seen\ by\ I_N}$

② 가능한 작은 값의 R 사용

③ I_{os} 가 작은 op amp 사용.

5.3 Low-Input-Bias-Current op amp.

* Superbeta-Input op amp
  - LM308 (NS)
  - $I_B \simeq 1$ nA or less

* Input-Bias-Current Cancellation
  - OP-07 (AD)
  - $I_B = \pm 1$ nA, $I_{os} = 0.4$ nA

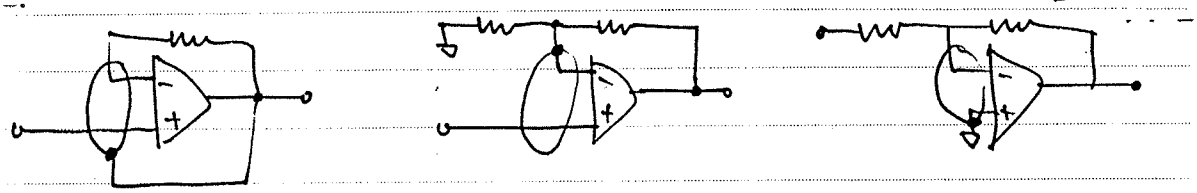
* JFET-Input op amp.
  - LF 356 : bi FET op amp (NS)
    $I_B = 30$ pA, $I_{os} = 3$ pA
  - AD549 (AD), OPA129 (BB)
    $I_B < 100$ fA

- Applications : electrometer, ion gauge, photodetector (이온 게이지, 광검출기)

* MOSFET - Input Op Amp.
  - TLC 279 : CMOS op amp, (TI)
    $I_B = 0.7\ pA$, $I_{os} = 0.1\ pA$

* Input Bias-Current Drift : Fig 5.9
  - BJT : T↑ ⇒ I_B↓
  - FET : T↑ ⇒ I_B↑

* Input Guarding : Fig 5.10
  - Guard ring minimizes leakage current across PCB
  - Use Teflon sockets if any



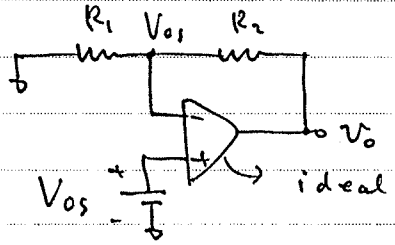
5.4 Input Offset Voltage : Fig 5.11

- $v_o = a(v_p - v_N) \neq 0$ for $v_p = v_N$ (≠0)
- $v_o = a(v_p + V_{os} - v_N) = 0$, or
  $v_N = v_p + V_{os}$
  (V_{os} : input offset voltage)
  ($\rightarrow\ v_N \neq v_p$)

- V_{os} : mV ~ μV

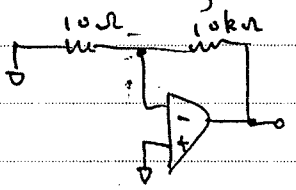
  - 741C : V_{os} = 2mV ~ 6mV
  - 741E : V_{os} = 0.8mV ~ 3mV
  - Op-77 : V_{os} = 10μV ~ 50μV
    - ↳ ultralow offset voltage op amp.

* Errors Caused by V_{os}

① 

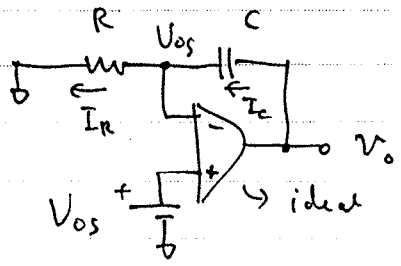
$$V_o = E_o = \left(1+\frac{R_2}{R_1}\right)V_{os}$$

- $\left(1+\frac{R_2}{R_1}\right)$: dc noise gain
- Measurement of V_{os}



$$V_o \Rightarrow V_{os} = \frac{V_o}{1001}$$

($R_1 // R_2$ 의 값은 I_B 의 영향을 줄이기 위함)

② 

$$I_c = I_R = \frac{V_{os}}{R}$$

$$V_o(t) = E_o(t) + V_o(0) = \frac{1}{RC}\int_0^t V_{os}\,d\xi + V_o(0)$$

- ramp ⇒ op amp saturation

* Thermal Drift
  - $TC(V_{os}) = \frac{\partial V_{os}}{\partial T} \sim \mu V/^\circ C$
  - 741 : $TC(V_{os}) \sim 5\,\mu V/^\circ C$
  - Op-77 : $TC(V_{os}) \sim 0.1\,\mu V/^\circ C \sim 0.3\,\mu V/^\circ C$

$$V_{os}(T) \doteq V_{os}(25^\circ C) + TC(V_{os})_{avg} \times (T - 25^\circ C)$$

* CMRR
  - $V_o = a_{DM}(V_p - V_N) + a_{CM} V_{CM}$

$$\begin{cases} a_{DM}: \text{differential-mode gain} = a \\ a_{CM}: \text{common-mode gain} \\ V_{CM} = \frac{1}{2}(V_p + V_N) \end{cases}$$

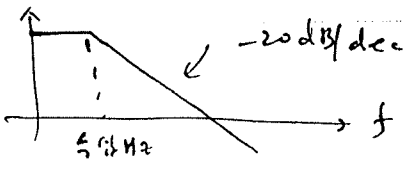
$$V_o = a_{DM}\left[V_p - V_N + \frac{a_{CM}}{a_{DM}} V_{CM} \right]$$

$$= a_{DM}\left[V_p + \underbrace{\frac{V_{CM}}{CMRR}}_{\text{↳ input offset voltage 차이}} - V_N \right]$$

$$(CMRR)^{-1} = \frac{\partial V_{os}}{\partial V_{CM}} = 10^{-CMRR_{dB}/20}$$

$$\left(CMRR_{dB} = 20 \log_{10} CMRR \right)$$

- 741 : $CMRR_{dB} = 70 \sim 90$ dB ↗ $(CMRR)^{-1}$: 31.6~316 μV/V
- Op-77 : $(CMRR)^{-1} = 0.1 \sim 1\,\mu V/V$
- $CMRR_{dB}$



- Since $v_N \approx v_p$, $v_{cm} \doteq v_p \doteq v_N$
- { Inverting amp ⇒ $v_p = 0$ ⇒ CMRR ≒ 무한대 에 가깝다.
  { IA ⇒ CMRR ≒ 무한대.

◎ Example 5.4

* PSRR (Power Supply Rejection Ratio)

- 전원 공급기 내부의 V_S 가 ΔV_S 변화

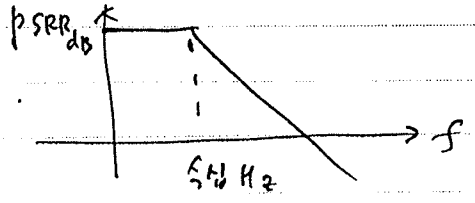
⇓

input offset voltage 변화

$$v_o = a\left[v_p + \frac{\Delta V_S}{PSRR} - v_N\right]$$

$$\frac{1}{PSRR} = \frac{\partial V_{OS}}{\partial V_S} \quad \text{in } \mu V/V$$

- PSRR : 80 ~ 120 dB
- 741 : $(PSRR)^{-1}$ = 30 ~ 150 uV/V
- OP-77 : $(PSRR)^{-1}$ = 0.7 ~ 3 μV/V



- 60Hz ripple or high-freq ripple in switching mode power supply

⇓

ΔV_S

⇓

V_{OS} ⇒ output noise (hum 등)

◎ Example 5.5

* Change of V_{os} with Output Swing
  - a is finite $\Rightarrow$ Δv_o produces $\Delta v_o/a$ at input

$$v_o = a\left[v_p + \underbrace{\frac{\Delta v_o}{a}}_{\hookrightarrow \Delta V_{os}} - v_N\right]$$

Summary:

$$V_{os} = \underbrace{V_{os_0}}_{\hookrightarrow \text{initial input offset voltage}} + TC(V_{os})\Delta T + \frac{\Delta v_p}{CMRR} + \frac{\Delta V_s}{PSRR} + \frac{\Delta v_o}{a}$$

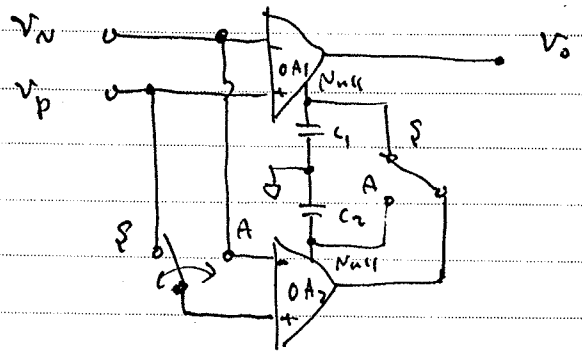
@ Example 5.6

5.5 Low-Input-Offset-Voltage Op Amp.

* Bipolar Op Amp
  - op-27E (AD) : $V_{os} = 10\mu V \sim 25\mu V$
    $TC(V_{os}) = 0.2\mu V/^\circ C \sim 0.6\mu V/^\circ C$

* FET-Input Op Amp
  - AD547L (AD) : $V_{os} = 250\mu V$
    $TC(V_{os}) < 1\mu V/^\circ C$
  - OPA627B (BB) : $V_{os} = 40\mu V$
    $TC(V_{os}) = 0.4\mu V/^\circ C$
  - LT1055A (LT) : $V_{os} = 50\mu V$
    $TC(V_{os}) = 1.2\mu V/^\circ C$

* Chopper-Stabilized Op Amp (CSOA)
- Auto-zero op amp.



{ S : sampling
A : auto-zero
Switching : 수 kHz ~ MHz
↓
internal oscillator

- Auto-zero mode : OA_2 자체의 V_{OS2} 보상
- Sampling mode : OA1 의 V_{OS1} 보상.

- LTC1050 (LT) : $V_{OS} = 0.5\,\mu V$, $TC(V_{OS}) = 0.01\,\mu V/^\circ C$
- MAX420 (Maxim) : $V_{OS} = 1\,\mu V$, $TC(V_{OS}) = 0.02\,\mu V/^\circ C$

↑ - Switching noise, freq. aliasing problem

5.6 Input Offset-Error Compensation

①

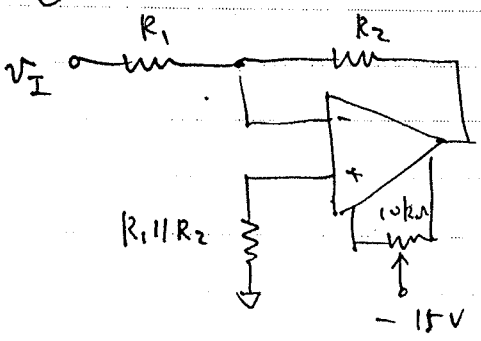


Fig 5.17 (a) 보상
(b) 비보상

$$v_o = A_S v_I + E_o$$

$$E_o = \left(1+\frac{R_2}{R_1}\right)\left[V_{OS} - (R_1 \| R_2) I_{OS}\right]$$

$$= \frac{1}{3} E_I$$

$$A_S = -\frac{R_2}{R_1} \quad \text{or} \quad 1+\frac{R_2}{R_1}$$

↳ signal gain

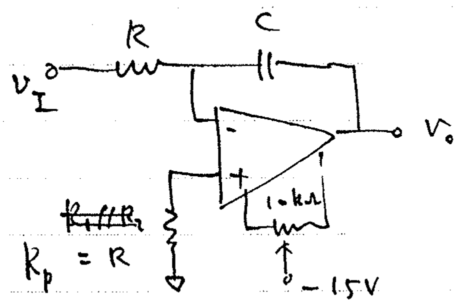
$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}$$

" V_{os}와 I_{os}의 효과를 다루며 회로의 차이로 제거할 것. "

$$E_I = V_{os} - (R_1 /\!/ R_2) I_{os}$$: total offset error refered to the input

E_o : total offset error referred to the output

②



$$v_o(t) = -\frac{1}{RC}\int_0^t \left[v_I(\xi) + E_I \right] d\xi + v_o(0)$$

$$E_I = R\, I_{os} - V_{os}$$

* Internal Offset Nulling

- External trimmer : 입력 단에 의도적으로 불균형을 만듦.
  (Fig 5.3 의 10kΩ 가변 저항)

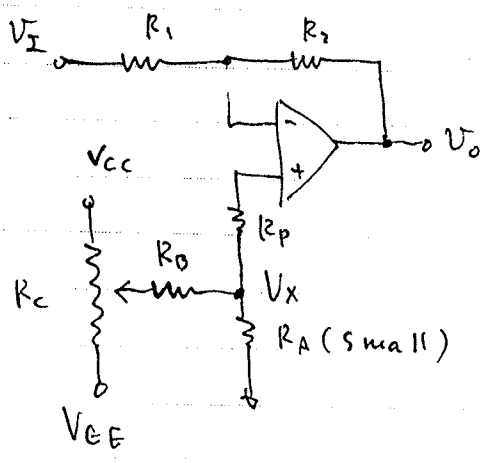
- Calibration : ① set $v_I = 0$
  ② Adjust trimmer for $v_o = 0$

- Dual or quad op amp package는 internal nulling 기능을 제공하지 않음 (∵ pin 수의 제한)

  ⇓

  trimmer를 이용하여 internal nulling을 하려면 그러한 pin을 제공하는 op amp를 이용.

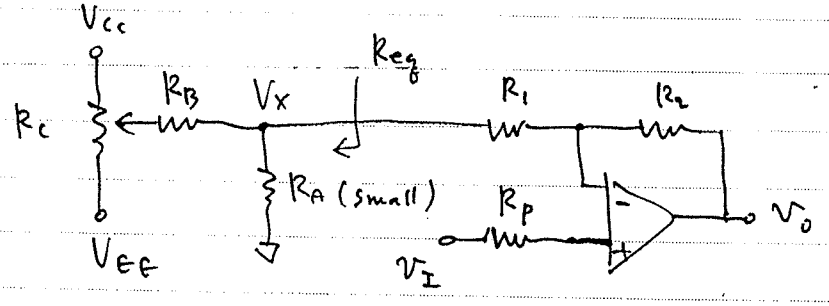
* External Offset Nulling
  - 외부에서 저항 추가해 주는 nulling.
  - CMRR, PSRR, drift 등에는 영향을 미치지 않음.



(Integrator 인 경우는 R_2 대신 C)

$R_B \gg R_C$
$R_A \ll R_P$

- calibration ① $V_I = 0$
  ② Adjust R_B for $V_o = 0$

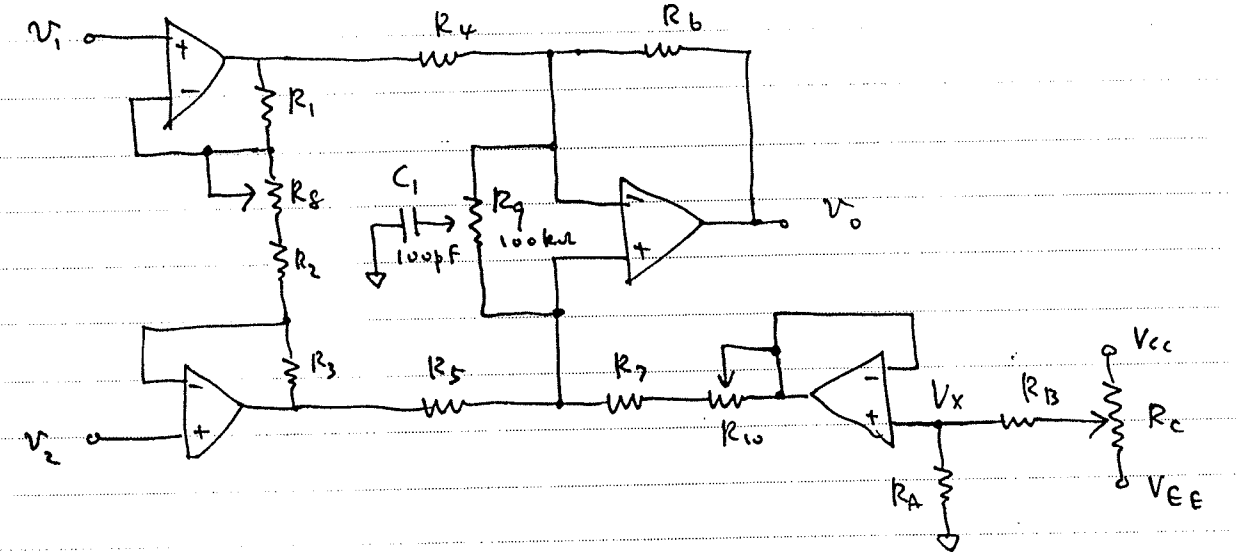


$R_{eq} \ll R_1$

$R_A \ll R_B \Rightarrow R_{eq} \simeq R_A$

$$A_f = 1 + \frac{R_2}{R_{eq} + R_1}$$

④ 3-op amp IA



① V_1 and V_2 = 0 (grounded) 시켜서
R_C 는 조절하여 $V_o = 0$

② R_8 은 조절하여 A_{DM} 은 반으로 ……

③ $V_1 = V_2 = V_I$, $-10V \le V_I \le 10V$ 시켜서
V_o 가 최소가 되도록 R_{10} 조절 (max. dc CMRR)

④ $V_1 = V_2 = V_I$, V_I = 제일 작은 값 시켜서
V_o 가 최소가 되도록 R_9 는 조절.
(이때 10kHz 정현파의 C_1 는 100pf 사용
C_1 은 고주파 CMR에서는 short 로 최소가 되도록 함)

AC CMRR

5.7 Maximum Ratings

- operating Temp { Commercial range : 0 ~ 70°C
  industrial " : −25 ~ 85°C
  military " : −55 ~ 125°C

DATE

* Absolute Maximum Ratings
- If exceeded, permanent damage.

- Maximum supply voltages
- Maximum differential-mode input voltages
- " common-mode " "
- Maximum internal power dissipation (P_{max})

* Input Voltage Range
- input voltage range for normal operation
- Single-supply op amp (V_{ss} − 1.5 V ~ 0 V) : LM324 (NS)

* Output Voltage Swing
- $V_{OL} \leq V_o \leq V_{OH}$
- rail-to-rail op amp : LMC 6464 (NS)
  ↳ $V_{EE} \leq V_o \leq V_{CC}$

* Overload Protection

- I_{sc} : output short-circuit current
- 741 : $I_{sc} \doteq 25$ mA
- power op amp
  PA04 (Apex Microtechnology) : 20 A
  OPA501 (BB) : 10 A

H/W : 5.2, 5.7, 5.10, 5.12, 5.23, 5-29