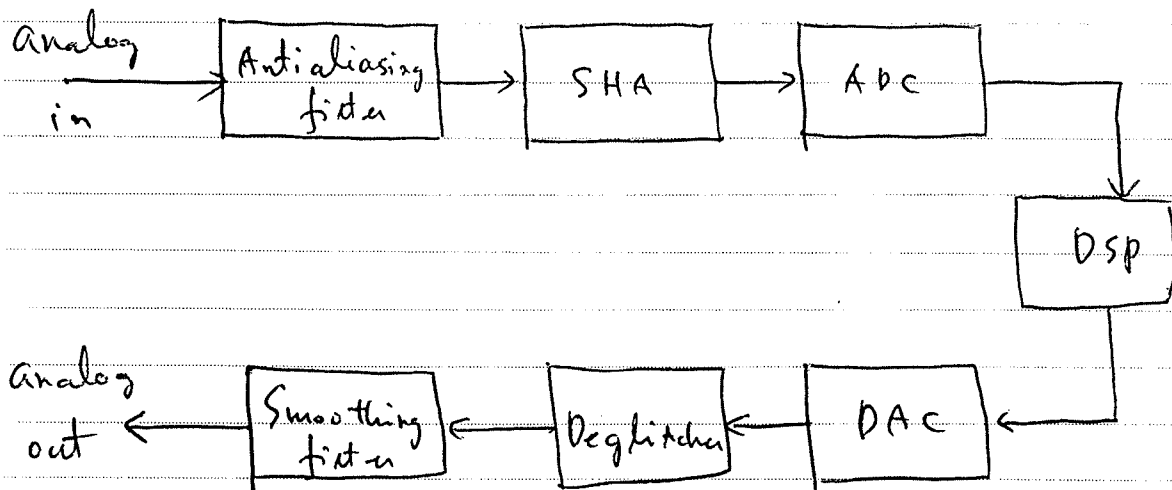


## Chapter 12 D/A and A/D Converter

\* Sampled data system



### 12.1 Performance Specifications

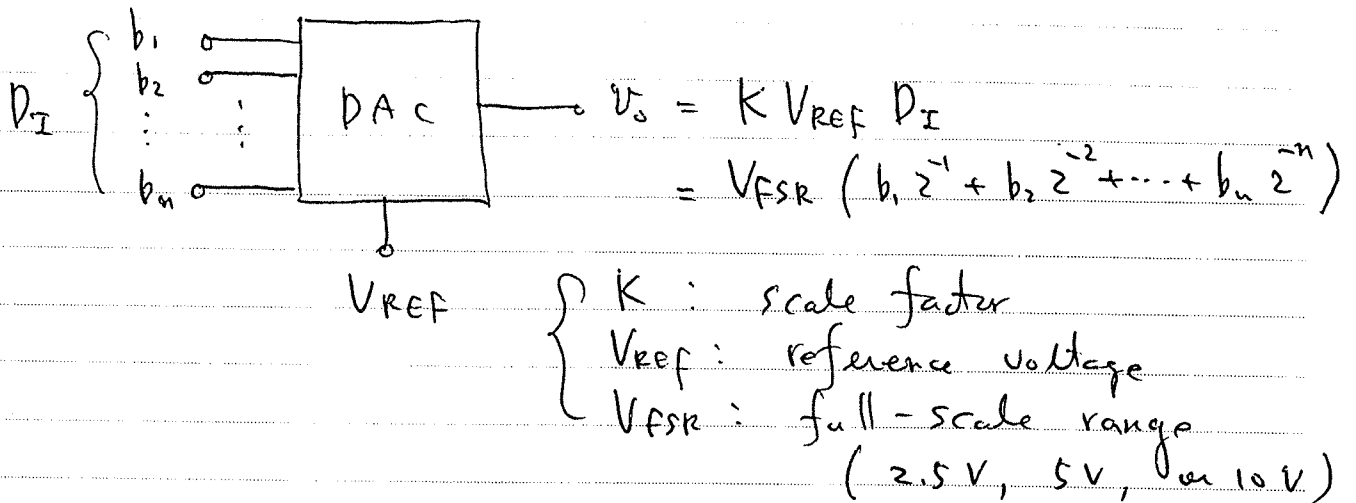
$b_1, b_2, \dots, b_n$  :  $n$ -bit word  
↑                    ↑  
MSB                LSB

$D = b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}$  : fractional binary value

2/2

$D = b_1 2^{n-1} + b_2 2^{n-2} + \dots + b_n 2^0$  : decimal value

## \* DAC



Current output  $I_o$  :

$$I_o = K I_{REF} D_I = I_{FSR} D_I$$

( $I_{FSR} = 1.0 \text{ mA}$ , typically)

$V_{REF}$  is  $2^m$  bits : MDAC (multiplying DAC)

$$\left\{ \begin{array}{l} \text{Resolution} = V_{FSR} / 2^n = \text{LSB} \\ \text{Dynamic range} = \text{DR} = 20 \log_2 2^n \\ V_{FSV} = \text{full-scale value} = (1 - 2^{-n}) \times V_{FSR} \end{array} \right.$$

Ex) (2-bit DAC,  $V_{FSR} = 10 \text{ V}$ )

$$\left( \begin{array}{l} \text{Resolution} = \text{LSB} = \frac{10}{2^{12}} = 2.44 \text{ mV} \\ V_{FSV} = (1 - 2^{-12}) \times 10 = 9.9976 \text{ V} \\ \text{DR} = 72.25 \text{ dB} \end{array} \right.$$

© Fig 12.3 (p 517) : offset error and gain error

## \* DAC Specifications

$$\left. \begin{array}{l} \text{Absolute accuracy} = \left| \text{Actual output} - V_{FSR} D_I \right|_{\max} \\ \text{Absolute accuracy} \approx \frac{1}{2} \text{LSB} \text{ of } (4\%) \end{array} \right\}$$

Static error  $\left\{ \begin{array}{l} \text{offset error} \\ \text{gain error} \end{array} \right\}$  Fig 12.3

$\left\{ \begin{array}{l} \text{Integral nonlinearity (INL)} = \text{relative accuracy} \\ \text{Differential nonlinearity (DNL)} \end{array} \right\}$

Dynamic error

- Settling time =  $t_s$  (band =  $\pm \frac{1}{2}$  LSB)

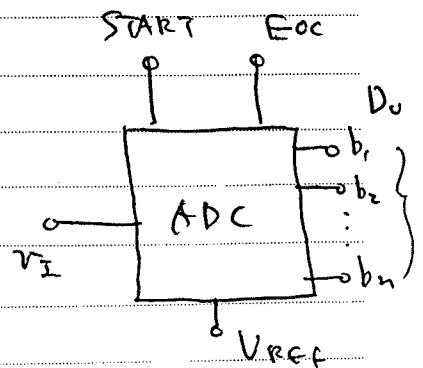
$\sim 10 \text{ ns} \sim 10 \mu\text{s}$

- Glitch : spikes at the output

## \* ADC

$$D_o = b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}$$

$$= \frac{V_I}{K V_{REF}} = \frac{V_I}{V_{FSR}}$$



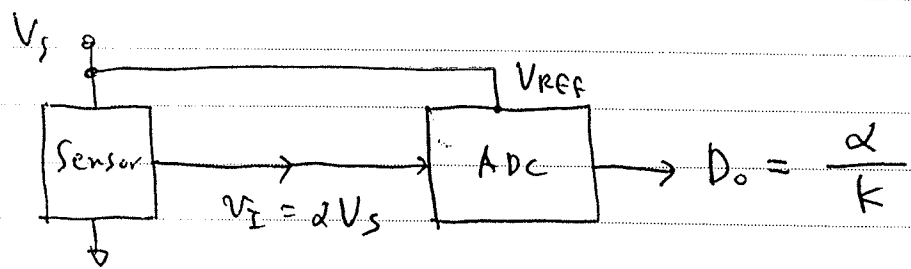
Control signals

$\left\{ \begin{array}{l} START : \text{start of conversion} \\ EOC : \text{end of conversion} \end{array} \right.$

Output } parallel  
          } serial

μP interface } latch  
                  } buffer (3-state)  
                  } control logic

⊙ Ratio metric conversion



⇒ Reference independent conversion  
   { high accuracy from moderate reference

⊙ Fig 12.5 : 3-bit ADC,  $V_{FSR} = 1V$

⊙ n-bit ADC

- code ranges =  $2^m$  intervals  
   (711) 3-bit ADC ⇒ 011 (code)

$V_{FSR} = 1V$ ;  $V_I : \frac{3}{8} \pm \frac{1}{16} V$

- Quantization error or quantization noise

⇒  $e_q = \pm \frac{1}{2} LSB$

(  $n \uparrow \Rightarrow e_q \downarrow$  )

Fig 12.5 (b)  $e_q = \frac{V_{FSR}}{2^n \sqrt{12}}$

(\*)  $v_i$  is sinusoidal,  $v_{i, max} = \frac{V_{FSR}}{2}$  (for max. SNR)

$$SNR_{max} = 20 \log_{10} \frac{\frac{V_{FSR}}{2} / \sqrt{2}}{V_{FSR} / 2^n \sqrt{12}}$$

$$= 6.02n + 1.76 \text{ dB}$$

( $n \uparrow \Rightarrow SNR \uparrow$ )

\* ADC Specifications

- offset error
- Gain error
- Differential nonlinearity
- Integral nonlinearity
- Stability.

Conversion time :  $< 1 \mu s \sim 5 \mu s$

$$ENOB = \frac{S/(N+D) - 1.76 \text{ dB}}{6.02}$$

effective number of bits

$S/(N+D)$  : Signal-to-noise-plus-distortion ratio

$$\frac{S}{N+D}$$

## 12.2 D/A Conversion Technique

### \* Weighted-Resistor DAC

Fig 12.7 (p 572)

$$V_o = -\frac{R_f}{R} V_{REF} (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n})$$

- Large resistance spread  $\left. \begin{array}{l} \text{---} \\ \text{---} \end{array} \right\} \frac{1}{2^{2n-2}}$
- Switch resistance
- b-bit DAC often a avg.

### \* Weighted-Capacitor DAC

Fig 12.8 (p 573)

- Wide capacitance spread.
- 10 bit ~~1 bit~~

### \* Potentiometric DAC

Fig 12.9 (p 573)

- Large number of resistors
- 8 bit ~~1 bit~~

### \* R-2R Ladder

- Fig 12.12 (p 577)
- Most popular

### \* Bipolar DAC

### 12.3 MDAC Applications

\* MDAC : Fig 12.22 (p 587) , R-2R ladder

#### \* Applications

- Digitally programmable attenuator (Fig 12.23)
- " " amplifier (Fig 12.23)
- " " filter (Fig 12.24)
- " " oscillator (Fig 12.25)

### 12.4 A/D Conversion Techniques

\* DAC - Based ADC : Fig 12.26 (p 591)

⊛ Successive - Approximation ADC (SA ADC) ;  
Fig. 12.28 (p 593)

⊛ Charge Redistribution ADC (CR ADC) ;  
Fig. 12.29 (p 594)

⊛ Flash ADC : Fig 12.31 (p 596)

\* Subtracting ADC : Fig 12.32 (p 597)

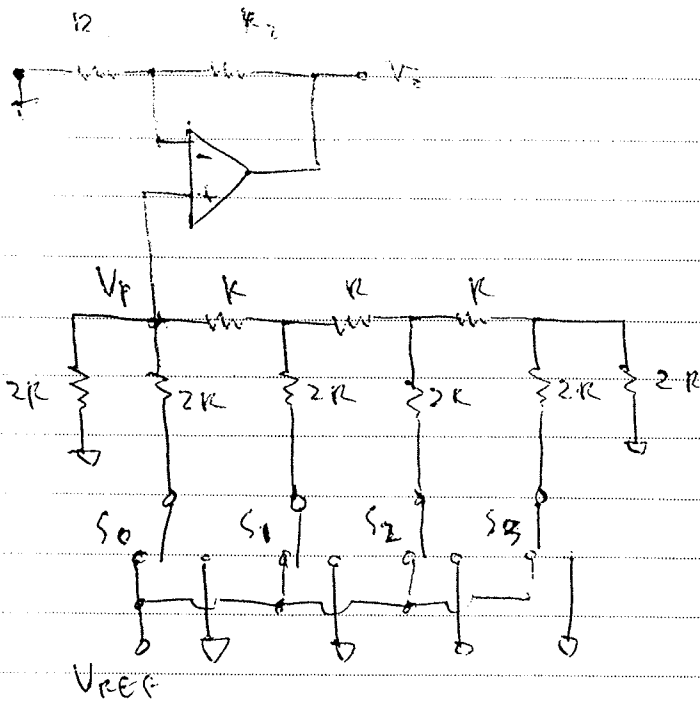
\* Pipelined ADC : Fig 12.33 (p 598)

\* Integrating - Type ADC : Fig 12.34 (p 599)

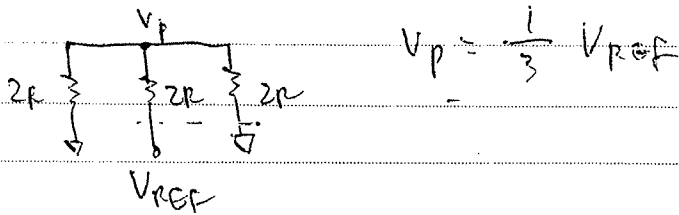
12.5 Oversampling Converters ( $\Sigma-\Delta$  ADC)

\* Nyquist - Rate Sampling.

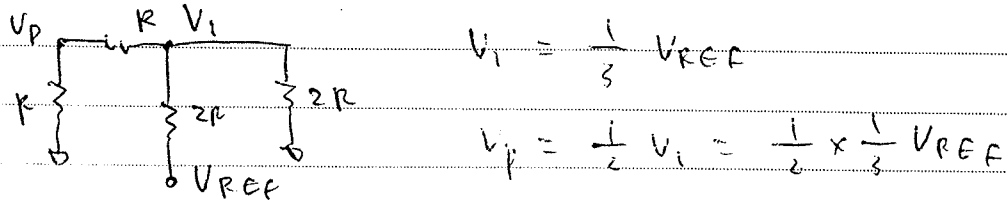




(i)  $S_0$  ON (i.e.  $V_{REF}$ )



(ii)  $S_1$  ON



(iii)  $S_2$  ON

